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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
LI, AIMEE J	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID JOHN BUTCHER, STEPHEN JOHN HILL, and WILCO DIJKSTRA

Appeal 2009-010086[1]
Application 10/807,499[2]
Technology Center 2100

Before JOSEPH L. DIXON, STEPHEN C. SIU, and JAMES R. HUGHES, *Administrative Patent Judges.*

HUGHES, *Administrative Patent Judge.*

DECISION ON APPEAL[3]

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[1] An oral hearing was held in this appeal on August 11, 2010.
[2] Application filed March 24, 2004. The real party in interest is ARM Limited. (App. Br. 1.)
[3] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal from the Examiner's rejection of claims 1-48 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' Invention

Appellants invented an apparatus and method for processing data utilizing processing logic to perform the data processing, and an instruction decoder to decode program instructions to control the processing logic as specified by the program instructions. The decoder being responsive to a "compare and branch instruction" to: perform a comparison between a first value stored in a first register and a second value stored in a second register; copy, based on the comparison, a program counter value into a third register; determine a target branch address from a pre-programmed stored value and the program counter value; and branch to a sub-routine at the target branch address based upon a result of the comparison. In particular, the target branch address of a compare and branch instruction may be determined from a pre-programmed stored value rather than being calculated from a relative address specified within the instruction itself, allowing greater flexibility in the range of addresses that may be specified for the target branch address. (Spec. 3, ll. 11-31.)[4]

[4] We refer to Appellants' Specification ("Spec."); Appeal Brief ("App. Br.") filed July 21, 2008; and Reply Brief ("Reply Br.") filed March 5, 2009. We also refer to the Examiner's Answer ("Ans.") mailed January 7, 2009.

Representative Claim

Independent claim 1 further illustrates the invention. It reads as follows:

> 1. Apparatus for processing data comprising:
>
> processing logic operable to perform data processing operations; and
>
> an instruction decoder for decoding program instructions to control said processing logic to perform data processing operations specified by said program instructions, wherein said instruction decoder, in response to a compare and branch instruction, comprises a decoder for:
>
> (i) performing a comparison between a first value stored in a first register and a second value stored in a second register;
>
> (ii) copying, in dependence upon a result of said comparison, a program counter value to a third register;
>
> (iii) determining a target branch address from a pre-programmed stored value and said program counter value; and
>
> (iv) branching to a sub-routine at said target branch address in dependence upon a result of said comparison.

References

The Examiner relies on the following references as evidence of unpatentability:

Schmidt	US 5,727,227	Mar. 10, 1998
Ishizaki	US 6,484,314 B1	Nov. 19, 2002

ANDREW S. TANENBAUM, STRUCTURED COMPUTER ORGANIZATION, 10-12 (Prentice-Hall, Inc. 2nd ed. 1984) (hereinafter "Tanenbaum").

JOHN L. HENNESSY ET AL., COMPUTER ORGANIZATION AND DESIGN *The Hardware/Software Interface*, 410-16 (Julie Pabst ed., Morgan Kaufmann Publishers, Inc. 2nd ed. 1998) (1997) (hereinafter "Hennessy").

RANDALL HYDE, THE ART OF ASSEMBLY LANGUAGE PROGRAMMING, Chapters: Table of Contents; Chapter 6 Part 2 & Part 5 (1996), *available at* http://www.arl.wustl.edu/~lockwood/class/cs306/books/artofasm/toc.html (hereinafter "Assembly Language Programming").

WIKIPEDIA, THE FREE ENCYCLOPEDIA (2003) (search term: protected mode), http://en.wikipedia.org/wiki/Protected_mode (hereinafter "Wikipedia").

FREE ON-LINE DICTIONARY OF COMPUTING, FOLDOC, (1995-1999) (search terms: central processing unit; arithmetic and logic unit; control unit; machine cycle; and operating system), http://foldoc.org/ (hereinafter "FOLDOC").

Rejections on Appeal

The Examiner rejects claims 1-5, 7, 9-11, 13-17, 19, 21-23, 25-29, 31, 33-35, 37-41, 43, and 45-47 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ishizaki and Hennessy.

The Examiner rejects claims 6, 18, 30, and 42 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ishizaki, Hennessy, and Assembly Language Programming.

The Examiner rejects claims 8, 20, 32, and 44 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ishizaki, Hennessy, and Schmidt.

The Examiner rejects claims 12, 24, 36, and 48 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ishizaki, Hennessy, and Wikipedia.

ISSUE

Based on our review of the administrative record, Appellants' contentions, and the Examiner's findings and conclusions, the pivotal issue before us is as follows:

Does the Examiner err in finding the Ishizaki and Hennessy references would have collectively taught or suggested a decoder: performing a comparison between a first value stored in a first register and a second value stored in a second register, copying a program counter value to a third register based on the comparison result, determining a target branch address from a pre-programmed stored value and the program counter value, and branching to a sub-routine at the target branch address based on the result of the comparison?

FINDINGS OF FACT (FF)

Ishizaki and Hennessy References

1. We adopt as our own the Examiner's findings with respect to the Ishizaki and Hennessy references set out in the Answer. (Ans. 3-5, 15-19.)

ANALYSIS

Appellants contend that the Ishizaki and Hennessy references do not render independent claims independent claims 1, 13, 25, and 37 obvious. (App. Br. 10-15.) Specifically, Appellants contend that the Examiner has failed to present a "*prima facie* case of obviousness" because Ishizaki does not teach or suggest the features of "'copying,' 'determining' and

'branching,'" and Hennessy does not teach or suggest "'copying' or 'branching'" based on (in conjunction with) "the 'comparison.'" (App. Br. 11.) After reviewing the record on appeal, we agree with Appellants that the Ishizaki and Hennessy references would not have collectively taught or suggested the disputed features for essentially the reasons argued by Appellants.

The Examiner admits that the Ishizaki reference does not explicitly teach "copying, in dependence upon a result of said comparison, a program counter value to a third register, and for determining a target branch address from said program counter value." (Ans. 4.) The Examiner finds that Ishizaki teaches "branching on an exception and exception handling" (Ans. 5), but admits that Ishizaki doesn't teach "how exception handling affects the program counter" (*id.*). The Examiner relies on Hennessy to cure these deficiencies, finding that Hennessy describes "copying, in dependence upon a result of said comparison, a program counter value to a third register, and for determining a target branch address from said program counter value." (Ans. 5.)

The Examiner asserts that Hennessy teaches determining a branch target address from a program counter (Ans. 5, 16), but the Examiner does not describe how the teaching of Hennessy – determining a branch target address from a program counter – and the purported teaching of Ishizaki – determining a branch target address from a stored value (Ans. 4) – may be combined to teach determining a branch target address from a program counter and a stored value. As pointed out by Appellants, the Examiner does not explain how the copying, determining, and branching functionality purportedly taught by Hennessy (Ans. 5, 16) relates to the comparison and

branching purportedly taught by Ishizaki. (App. Br. 10-11, 13; Reply Br. 2-4.) Rather, the Examiner simply concludes that:

> A person of ordinary skill in the art at the time the invention was made, and as taught by Hennessy, would have recognized that copying the program counter value and determining a target branch address from the program counter value allows the operating system to take the appropriate action to report and correct the error then restart execution of the program (Hennessy page 411).

(Ans. 5.)

Thus, we are constrained by the record before us to find that the combination of the Ishizaki and Hennessy references fails to teach or suggest at least one of the disputed features. Neither reference describes, and the reference combination does not teach or suggest, a decoder that performs the functions of determining a target branch address from a pre-programmed stored value and a program counter value, and branching to a sub-routine at the determined target branch address based on a result of a comparison. Consequently, we find the Examiner has not presented a prima facie obviousness rejection with respect to Appellants' independent claim 1. Appellants' independent claims 13, 25, and 37 include limitations of commensurate scope. Appellants' dependent claims 2-5, 7, 9-11, 14-17, 19, 21-23, 26-29, 31, 33-35, 38-41, 43, and 45-47 depend on their respective base independent claims 1, 13, 25, and 37. Accordingly, we reverse the Examiner's obviousness rejection of claims 1-5, 7, 9-11, 13-17, 19, 21-23, 25-29, 31, 33-35, 37-41, 43, and 45-47.

The Examiner rejects claims 6, 8, 12, 18, 20, 24, 30, 32, 36, 42, 44, and 48 under § 103 over Ishizaki and Hennessy in further combination with several prior art references: claims 6, 18, 30, and 42 over Ishizaki, Hennessy,

and Assembly Language Programming; claims 8, 20, 32, and 44 over Ishizaki, Hennessy, and Schmidt; and claims 12, 24, 36, and 48 over Ishizaki, Hennessy, and Wikipedia. Appellants' dependent claims 6, 8, 12, 18, 20, 24, 30, 32, 36, 42, 44, and 48 depend on their respective base independent claims 1, 13, 25, and 37. As set forth *supra*, we find that the combination of the Ishizaki and Hennessy falls short of disclosing, teaching, or suggesting at least one of the disputed features of claims 1, 13, 25, and 37. None of the Assembly Language Programming, Schmidt, and Wikipedia references cures these noted deficiencies. Consequently, we are constrained by the record before us to find that the Examiner's cited prior art combinations of Ishizaki and Hennessy with Assembly Language Programming, Schmidt, and Wikipedia do not collectively teach or suggest the disputed limitations of Appellant's claims 6, 8, 12, 18, 20, 24, 30, 32, 36, 42, 44, and 48. It follows that Appellants have shown that the Examiner erred in finding that the cited prior art combinations of Ishizaki and Hennessy with Assembly Language Programming, Schmidt, and Wikipedia render Appellant's claims 6, 8, 12, 18, 20, 24, 30, 32, 36, 42, 44, and 48 obvious. Accordingly, we reverse the Examiner's obviousness rejection with respect to these claims.

CONCLUSIONS OF LAW

Appellants have shown that the Examiner erred in rejecting claims 1-48 under 35 U.S.C. § 103(a).

DECISION

We reverse the Examiner's rejections of claims 1-48 under 35 U.S.C. § 103(a).

REVERSED

llw

Nixon & Vanderhye, PC
901 North Glebe Road, 11th Floor
Arlington, VA 22203